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Greener SiC wafers with Smart Cut technology

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SiC membrane supports record-breaking modulation rates for telecom lasers

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A greener SiC wafer with Smart Cut technology

Smart Cut substrate technology charts a greener, faster and better path for the production of power electronic components

BY OLIVIER BONNIN, ERIC GUIOT, WALTER SCHWARZENBACH AND GONZALO PICUN FROM SOITEC

THIS YEAR has witnessed horrendous flooding in China and central Europe, along with soaring temperatures in north America. So it would appear that climate change is already underway, driven by rising levels of CO_2 emissions. The prevailing view of the scientific community is that this situation is only going to deteriorate, and if the additional rise in temperature is not restricted to below 1.5 °C, our climate will undergo a substantial change.

Key to trimming CO_2 emissions and staying within that limit for a temperature rise is sustainable development, which includes the introduction of greener technologies and processes. The industrial sector,

electricity generation and transportation now accounts for about three-quarters of all CO_2 gas emissions. So there is clearly a need to build a better, greener energy ecosystem. This can be realized by making substantial improvements on three fronts: slashing the energy consumed by data-centres, ramping renewable energy production, and accelerating the production of zero emission vehicles (ZEVs).

Within the ZEV sector, efforts must be directed at taking every opportunity to increase the power conversion efficiency, from electrical generation through to the provision of power at the powertrain. To excel in this endeavour, there must be a shift towards the use of greener power electronic components that deliver better performance and are made from more eco-friendly production processes.

Today's incumbents, which are silicon-based components, are operating at their theoretical limit and cannot deliver the additional performance required for the more-efficient, greener systems needed for next-generation ZEVs. There must be a move to widespread adoption of wide bandgap semiconductors, such as SiC, which enable devices that combine higher operating temperatures with faster switching frequencies and higher efficiencies. Powertrains adopting this technology not only excel in efficiency – they are also smaller, lighter, and lower-cost.

Pioneering the uptake of SiC in ZEVs is Tesla. Back in 2017 it started deploying this technology in its Model 3 cars, importing power electronic components from STMicroelectronics. Where Tesla has led, others are sure to follow, creating a massive market for SiC, given that the ZEV market will account for more than half of all vehicle sales by the end of this decade, and all purchases come 2050 (see Figure 1).

Going hand-in-hand with this revolution in transportation, there needs to be a dramatic increase in renewable energy production. Humanity is heading in the right direction, with the installed capacity for producing energy from the sun and the wind expected to increase three-fold by 2040. In both these forms of renewable, the inverter is a key component.

Designers of this component are seeking reductions in volume and weight, alongside an increase in global system efficiency. To accomplish these goals, they will employ simplified bi-directional topologies, enabled by SiC, that handle more than 100 kW.

Hampering efforts to curb CO_2 emission is the rapid growth in the IoT (Internet of Things) and AI (Artificial Intelligence). They contribute to global emissions by digital applications, a sector estimated to account for up to 10 percent of all emissions by 2025, and possibly more than 20 percent by the end of this decade. There is an urgent need for new data centres with smaller CO_2 footprints. One way to realise this is to increase electrical power efficiency. For that, switching to a higher power density by introducing SiC is a valid option.

The Achilles heel of SiC

While SiC has many strengths, production of boules by the conventional technique, physical-vapour transport, requires temperatures of typically 2300°C to 2400 °C – this is far higher than that for silicon, which is grown at 1400 °C to 1500 °C. Additional drawbacks are that it can take a week to grow a SiC boule, and this only yields 40 to 50 wafers.

All these impediments help to explain why today's SiC wafers are up to 50 times the price of silicon equivalents, which are grown in just a few days. The environmental impact of SiC's production process has to be addressed, given that this material offers so much promise in helping to curb global CO_2 emissions.

Insights from Emmanuel Sabonnadière, Soitec's Vice President, Silicon Carbide

Q: What is Soitec's view on engineered substrate technology?

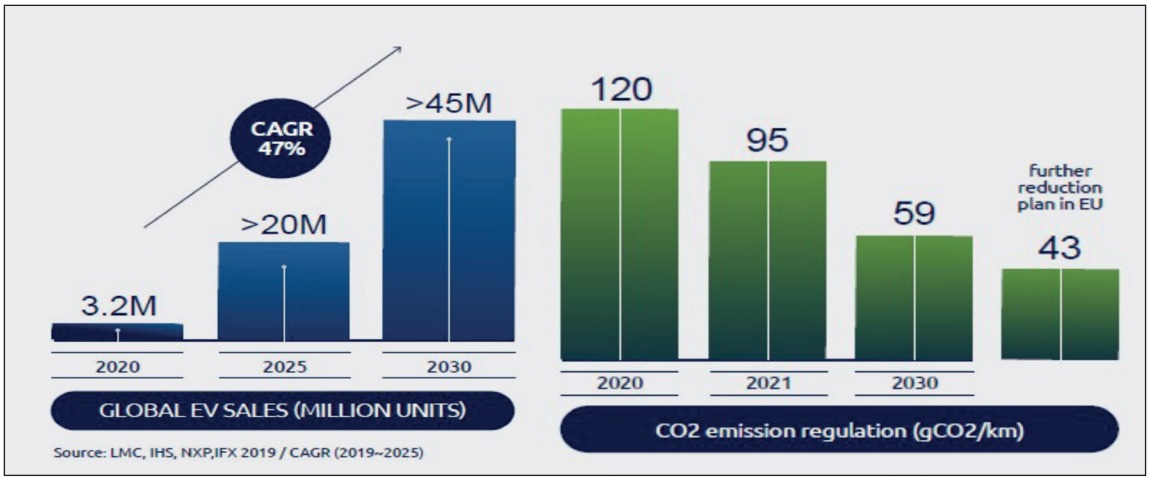
A: For the last thirty years, we have been successfully promoting the benefits and manufacturing engineered substrates in microelectronics. We are now exploring power electronics with a better, faster and greener path, based on advanced engineered substrates. Silicon carbide is the most promising material for power electronics, especially for the new electrical vehicles market. We are developing an alternative to classic bulk silicon carbide that has a very low environmental budget: Smart Cut silicon carbide. This combines our Smart Cut process, invented decades ago, with SiC materials. This greener technology is perfectly aligned with our efforts over the years at pioneering and leading engineered substrate technology.

Q: Are you increasing production of Smart-Cut silicon carbide?

A: Smart Cut silicon carbide is at the adoption phase, with some key players involved in the new booming electric-vehicle markets. Smart Cut silicon carbide will also find alternative markets, for applications requiring high-efficiency power conversion at 400-800-1200 volts, for powers of 75-150-300 kilowatts and more. We are expecting high single-digit growth over the coming years with our Smart Cut silicon carbide. This will provide us with a strategic diversification from microelectronics to automotive applications.

Q: How much money will you be investing in Smart-Cut silicon carbide production?

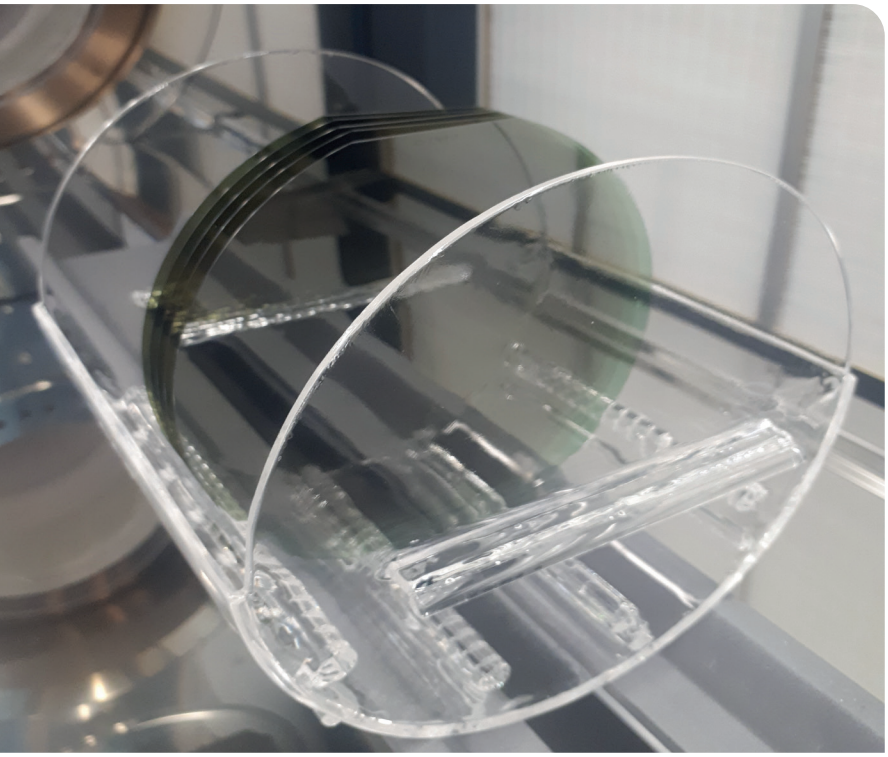
A: It depends on the strategic partnerships under construction. However, we estimate that our Capex investment in Smart Cut silicon carbide production over the next five years will be about 20 percent of our total investment over that period. We announced this intention in June at the *Soitec Capital Markets Day* (for details, see: https://www.soitec.com/media/images/Soitec-CMD_2021.pdf).



➤ Figure 1. The fast transition towards EVs will be a key factor behind reductions in CO_2 emissions. This transition will be accentuated by governmental regulations on gCO_2/km.

At Soitec of Bernin, France, we have a solution to this problem: a proprietary layer-splitting and wafer-bonding technology, known as Smart Cut. Applying this to SiC allows a thin, monocrystalline layer of this material to be transferred from a SiC donor substrate to a SiC carrier substrate.

Our Smart Cut technology is a cost-effective, environmentally friendly manufacturing technology that we employ to fabricate advanced engineered substrates. For more than thirty years we have used this technology to manufacture silicon-on-insulator wafers for microelectronics. Recently, we have also applied this technique to the production of piezoelectric materials and compound semiconductors. The production process that we employ requires two starting wafers, one referred to as the donor and the other the carrier. Preparation of the donor involves ion implantation, to create a cleavage plan at a defined depth. When preparing our donor and carrier wafers, we take into account surface roughness – minimising this is crucial to realising a higher performance with microelectronics. Our approach is highly eco-friendly, thanks to re-use of the donor wafer more than ten times.



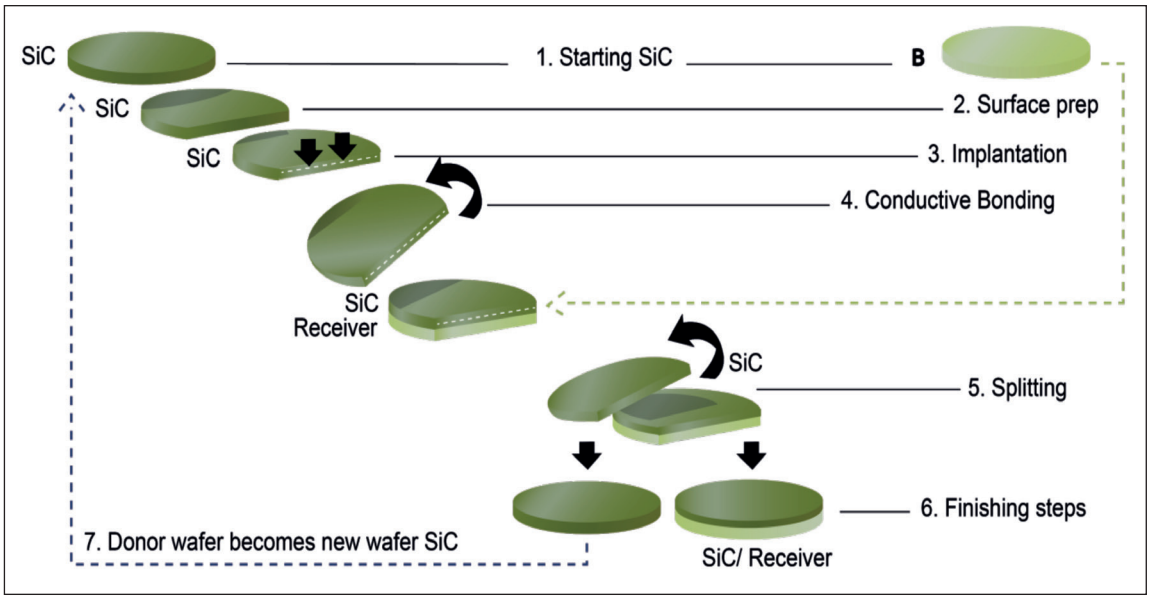
➤ Soitec's Smart Cut process, developed to reduce costs in the microelectronic industry, is poised to increase the competitiveness and volume of SiC devices.

When producing SiC substrates with our Smart Cut technology, we have found that optimisation of the bonding step is crucial for realising high levels of electrical and thermal conductivity. Our investigations have shown that the contribution of the bonding interface to the total substrate electrical resistance is equivalent to that of just a few tens of microns of standard SiC material. After Smart Cut splitting and transfer of a thin slice of SiC from the donor to the carrier substrate, we employ a finishing process that ensures that with polishing and anneal, our newly formed substrate is epi-ready and compatible with SiC device processing. Note that our Smart Cut SiC technology produces wafers with a top layer that is free from basal plane dislocations (see Figures 2 and 3).

Today, Smart Cut technology is used in microelectronics on wafers with diameters up to 300 mm, and we see no barrier to using this approach on larger-diameter SiC wafers. Thanks to this versatility, our Smart Cut SiC technology will accelerate the transition from 150 mm to 200 mm substrates while easing the ramp-up of volumes and securing availability for chip production. Another merit of the Smart Cut process is that for transposition to 200 mm SiC, it will be easier and faster to implement than it is for bulk SiC substrates.

Smart Cut's multiple benefits

There are significant benefits to making SiC devices from a Smart Cut wafer, rather than one produced from bulk SiC (see Figure 4 for a comparison of their construction). One merit is that when producing a device, the Smart Cut SiC substrate already includes the conversion buffer layer. This simplifies the drift epitaxy growth process.



➤ Figure 2. Soitec has adapted its Smart Cut process for the production of SiC.

Another attribute of Smart Cut SiC technology is that it offers an optimized top layer for device fabrication that features advanced physical properties and crystal quality from the SiC donor wafer, and is independent from the carrier material. This makes Smart Cut SiC technology so efficient and interesting for power electronics.

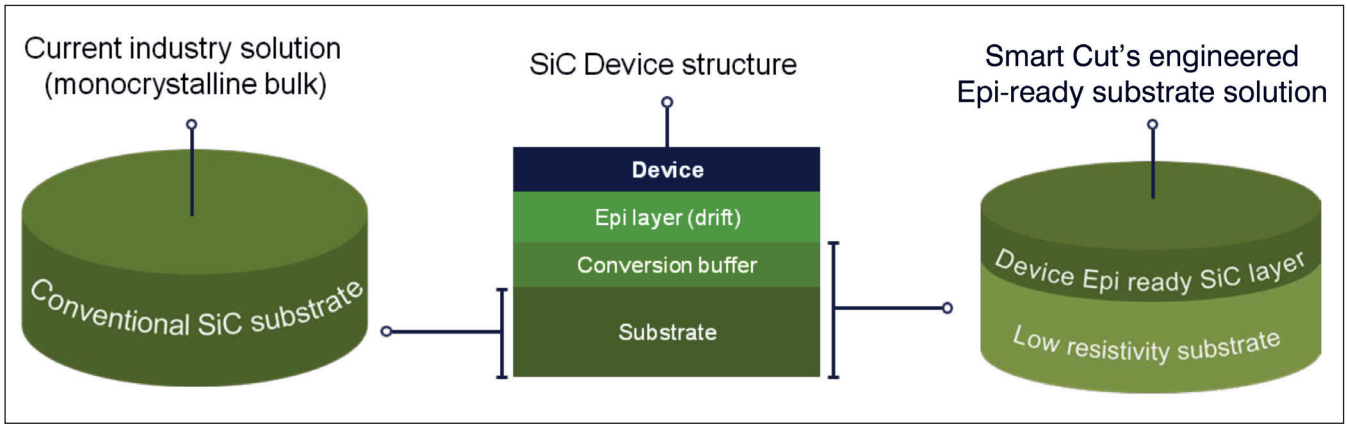
With substrates made from bulk SiC, there is a trade-off between electrical conductivity and crystal defectivity. If the doping level of 4H-SiC is increased, in order to reduce substrate resistivity, crystal defects increase. For *n*-type 4H-SiC wafers, the compromise involves a typical resistivity between 0.015 Ω cm and 0.025 Ω cm.

Thanks to material engineering of the base substrate, Smart Cut SiC decreases electrical resistivity of the substrate by at least a factor of four. This remarkable reduction of resistivity enables a shrinking of MOSFET dimensions by 5-15 percent, depending on device design. Yet another merit is that it might be possible to reduce or even skip wafer backgrinding. These savings on power electronics devices are substantial, enabling Smart Cut SiC technology to be considered as a powerful alternative to bulk SiC.

Additional strengths of Smart Cut SiC wafers are a high surface quality and reduced roughness, thanks to the specific engineering processes applied to the donor substrate and the transferred BPD-free top layer. These improvements drive down the induced epi-grown defect density, leading to a 20 percent increase in the yield of devices with dimensions above 20 mm².

In short, the disruptive approach of Smart Cut SiC technology lies in reusing, more than 10 times, a donor that is free from basal plane dislocations, and the provision of an ultra-smooth top layer on top of a low-resistivity receiver. As re-use allows a ten-fold increase in the number of dies produced, compared to a bulk SiC wafer, the introduction of Smart Cut SiC alleviates the supply chain, while reducing the environmental impact of producing boules.

➤ Figure 3. Pictures of bulk SiC (left), Smart Cut SiC (centre), and Smart Cut SiC with devices (right).



➤ Figure 4. A comparison of Smart Cut SiC and bulk SiC for SiC device fabrication.

Building better devices

Through collaboration with major European industrial and research and technology partners, we have fabricated junction barrier Schottky (JBS) diodes on our first-generation of Smart Cut SiC substrates, using a 20 mΩ cm resistivity carrier substrate. Electrical measurements on these devices reveal a performance equivalent to that of JBS diodes prepared on a reference bulk SiC wafer, which has been issued from the same batch of Smart Cut SiC donor (see Figure 5, left). Based on this result, it is clear that Smart Cut SiC wafers can fully replace bulk SiC for manufacturing power electronics devices.

We have modelled the transfer characteristics of this JBS diode, prepared on our Smart Cut SiC substrate. For this work, we considered the contributions of the measured electrical characteristics from the bonding interface and from the alternative, low-resistivity SiC carrier substrate. Calculations indicate that at a voltage of around 1.4 V, the current rating of this JBS diode increases by 20 percent (see Figure 5, right). This benefit will aid designers of power electronics components. They can design a product with a higher current rating, while keeping their existing design and technology; or they can shrink the total die area by more than 15 percent. As well as reducing die cost, the latter cuts switching losses by 10 percent, thanks to a reduced gate surface.

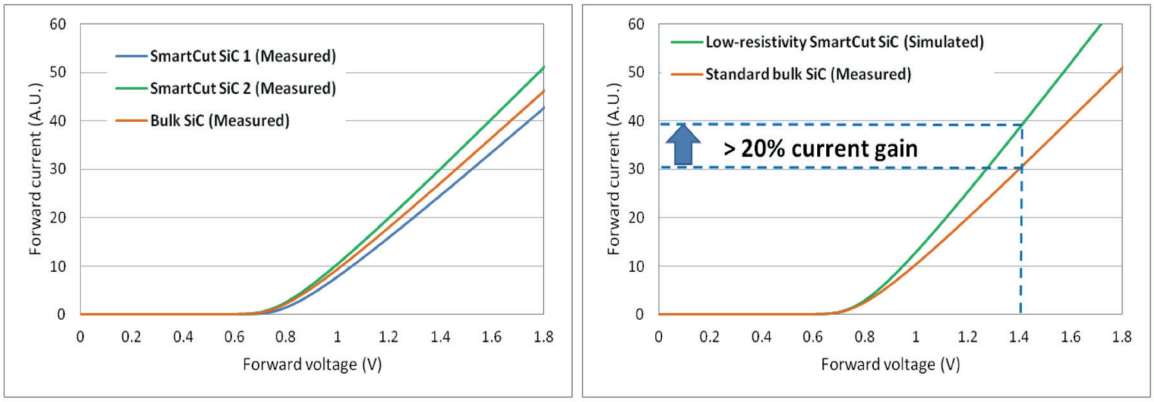
Cutting carbon footprints

When considering the environmental impact of the life cycle of power electronic devices, from raw materials preparation up to final components usage, the benefits of Smart Cut SiC technology are: a lower energy budget for SiC, thanks to multiple re-use of bulk SiC donors; and the adoption of a low resistivity handle wafer from a simpler, lower-energy manufacturing process. Note that the carrier substrate can be fabricated at lower temperatures – that is, below 1500 °C – with processing taking just one or two days. The upshot is an energy consumption close to that required to prepare a silicon wafer, which is a major breakthrough for SiC.

Using our Smart Cut SiC technology, 500 epi-ready wafers can be produced from SiC boules that yield 40-50 wafers with today's conventional SiC technology. This hike in efficiency by an order of magnitude is a great contributor to reducing the overall carbon footprint of SiC technology, which has a high environmental budget associated with SiC boule production.

As electric vehicle production soars throughout this decade, our technology will come to the fore by offering a reliable, disruptive alternative to bulk SiC that is currently utilized for the most advanced powertrain inverters.

The transformation of the automotive industry to more eco-friendly vehicles will include the implementation of evermore advanced SiC technology, which will be aided by the adoption of our Smart Cut SiC, a technology that improves performance and drastically cuts the carbon footprint associated with substrate production.



➤ Figure 5. Smart Cut SiC substrate performance.

Integra launches 100 volt RF GaN-on-SiC technology for defence

INTEGRA, a provider of RF and microwave power solutions, has introduced the industry's first 100 V RF GaN-on-SiC technology targeting a wide-range of applications including radar, avionics, electronic warfare, industrial, scientific and medical systems.

Operating at 100 V, this technology shatters RF power performance barriers by achieving 3.6 kW of output power in a single GaN transistor. Integra's 100V GaN gives designers the ability to dramatically increase system power levels and functionality while simplifying system architectures with less power combining circuitry compared to the more commonplace 50 V/65 V GaN technology. Customers ultimately benefit with a smaller system footprint and lower system cost.

Suja Ramnath, Integra's president and CEO, said: "Integra's 100 V RF GaN technology signifies a major milestone in the high-power market. This innovative technology removes the barriers limiting system performance today and allows new architectures previously not possible. We are excited that this disruptive technology will enable our customers to deliver a new generation of high-performance, multi-kilowatt RF power solutions while reducing their design cycle time and product costs."

Mahesh Kumar, an Aerospace and Defense radar systems architect and technology executive, said, "Integra's first to market 100 V RF GaN technology will completely redefine what's possible for high-power RF systems."

By delivering approximately two times the power compared to a 50 V GaN transistor in a single package, it will eliminate a significant number of combiners and associated electronic circuitry, resulting in lower system volume, weight and cost, and higher system efficiency.

Integra's first 100 V RF GaN product is the IGN1011S3600, designed specifically for avionics applications. The IGN1011S3600 delivers 3.6 kW of output power with 19 dB of gain and 70 percent efficiency. It is available for sampling to qualified customers.

Soitec appoints CEA-Leti CEO to head SiC programme

SOITEC, a Grenoble-based developer of innovative semiconductor materials, has appointed Emmanuel Sabonnadière, previously CEO of CEA-Leti, as new VP of its SiC programme, effective 1st July 2021. The newly created position reports to Bernard Aspar, COO and Head of Global Business Units at Soitec.

Microelectronic devices based on SiC substrates have numerous significant advantages. They boost the energy efficiency of existing and future automotive and industrial applications; they drive the electrification of vehicles, support the development of cutting-edge on-board chargers and charging stations, and enable the installation of advanced industrial renewable energy systems. Soitec's SmartCut SiC substrates are said to enable new levels of device performance and accelerate the adoption of SiC in automotive and other markets.

Before joining Soitec, Sabonnadière was CEO of CEA-Leti, a globally renowned technology research institute belonging to the French Alternative Energies and Atomic Energy Commission. Before, he served in executive positions at Philips Lighting (later called Signify), Gimv, a European investment firm, and General Cable Europe.

"With his profound experience in industry, business and technology, with his impressive global profile and his leadership skills, Emmanuel is a perfect fit for Soitec to drive our promising Smart Cut SiC technology and conquer new markets," said Bernard Aspar, COO and head of Global Business Units at Soitec. "Emmanuel has the intimacy with our local ecosystem and our customers worldwide to lead this development, launch manufacturing and drive the industrialisation of our SiC programme."

"I am excited and honored to join Soitec in this period of growth," said Sabonnadière. "Soitec's technology is a powerful motor to fuel new businesses and launch innovative and disruptive applications in the automotive and industrial markets. Soitec is well placed to capture the growing demand for smart semiconductor substrate solutions. I am looking forward to bringing Soitec's SiC solutions to market fruition quickly."