



SMART CUT™ TECHNOLOGY INVENTOR HONORED

Prestigious IEEE 2008 Cledo Brunetti Award Given to Michel Bruel of CEA-Leti

IEDM, San Francisco, CA — Decembre 16, 2008 — Soitec (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) wafers and other engineered substrates used in the microelectronics industry, reported that Dr. Michel Bruel is receiving today the *2008 Cledo Brunetti Award* during a ceremony at IEDM in San Francisco. As a former researcher of CEA-Leti, one of Europe's largest microelectronics research institutes, Dr. Michel Bruel is receiving this prestigious award for inventing the Smart Cut™ layer transfer technology that enabled widespread adoption of SOI for CMOS circuits, and the Soitec success story. Today, Smart Cut technology is supported by over 2000 patents worldwide owned both by CEA-Leti and Soitec, and accounts for 95% of all SOI production wafers.

Bruel's invention is a cost-effective process of atomic precision for slicing an ultra-thin layer and transferring it to another support. As such, it was the critical, pioneering step towards large-scale production of high-quality, high-volume SOI wafers. Today, the success of the Smart Cut technology can be attributed to its suitability for high-volume manufacturing; its inherent flexibility which enables substrates to be tailored to customer requirements; its scalability for future roadmap requirements; its applicability to any wafer diameter and material; and its use of standard IC manufacturing equipment.

The revolutionary nature of Bruel's breakthrough technology was first recognized by two of his colleagues: André-Jacques Auberton-Hervé and Jean-Michel Lamure, who were also CEA-Leti researchers and SOI experts. At this time in the early 1990's, Auberton-Hervé and Lamure had recently launched an SOI wafer-manufacturing start-up called Soitec in Grenoble using an older process technology. However, upon seeing Bruel's layer transfer process, Lamure and Auberton-Hervé contracted with Leti for an exclusive license. Trademarked as "Smart Cut™", the technology made its world debut in 1995, when Dr. Auberton-Hervé announced it at Semicon West.

"My colleagues at Soitec and throughout the industry join me to heartily congratulate Dr. Michel Bruel on winning the IEEE's Cledo Brunetti award," said Dr. André-Jacques Auberton-Hervé, President and CEO of the Soitec Group. "His invention of the Smart Cut technology paved the way for SOI wafers to become the starting material of choice for leading chipmakers, enabling them to better address key issues such as lowering power consumption and increasing performance."

"Leti has a strong tradition in advanced substrate innovation and engineering," said Dr. Laurent Malier, CEO of CEA-Leti. "As one of Leti's leading researchers, Michel Bruel invented what is now known throughout the industry as the Smart Cut technology. It is an excellent example of how fundamental research at a world-leading microelectronics laboratory can give birth to a game-changing technology on the worldwide stage. We warmly congratulate Dr. Bruel on his Cledo Brunetti award."

While the Smart Cut technology was first used for high-volume manufacturing of SOI wafers, it is a veritable toolbox for engineering new generations of advanced substrates. It has most recently been used for a new generation of advanced SOI substrates that support all the applications and architectures on the industry's sub-45 nm CMOS roadmap. For non-CMOS applications, Smart Cut™ enables a wide range of engineered substrates using silicon as well as other materials for a broad range of applications, including RF and microwave devices, analog, LEDs, MEMS, photonics, imaging, smart power, high-voltage and more.

The Cledo Brunetti Award was established in 1975 and is presented by the IEEE Board of Directors on the recommendation of the Technical Field Awards Council and the Awards Board, for outstanding contributions to miniaturization in the electronics arts. In the evaluation process, the following criteria are considered: innovation or development, social value, uniqueness of concept, other technical accomplishments, and the quality of the nomination. It may be presented each year to an individual or a team of not more than three. The award consists of a certificate and honorarium.

About the Soitec Group:

The Soitec Group is the world's leading innovator and provider of the engineered substrate solutions that serve as the foundation for today's most advanced microelectronic products. The group leverages its proprietary Smart Cut™ technology to engineer new substrate solutions, such as silicon-on-insulator (SOI) wafers, which became the first high-volume application for this proprietary technology. Since then, SOI has emerged as the material platform of the future, enabling the production of higher performing, faster chips that consume less power.

Today, Soitec produces more than 80 percent of the world's SOI wafers. Headquartered in Bernin, France, with two high-volume fabs on-site, Soitec has offices throughout the United States, Japan and Taiwan, and a new production site in the process of customers' qualification in Singapore.

Two other divisions, Picogiga International (Les Ulis) and Tracit Technologies (Bernin), complete the Soitec Group. Picogiga focuses on delivering advanced substrates solutions, including III-Vs epiwafers and gallium nitride (GaN)-based wafers, to the compound material world for the manufacture of high-frequency electronics and other optoelectronic devices. Tracit, on the other hand, focuses on thin-film layer transfer technologies used to manufacture advanced substrates for power ICs and microsystems, as well as generic circuit transfer technology for applications such as image sensors and 3D-integration. Shares of the Soitec Group are listed on Euronext Paris. For more information, visit www.soitec.com.

Soitec, Smart Cut and UNIBOND are trademarks of S.O.I.TEC Silicon On Insulator Technologies.

Press Contact:

Camille Darnaud-Dufour
Tel (France): +33 (0) 6 79 49 51 43
E-mail: camille.darnaud-dufour@soitec.com

###