



## SOITEC ANNOUNCES NEW GENERATION OF ADVANCED SUBSTRATES

*Solutions including ultra-thin SOI and ultra-thin BOX support the full range of applications and device architectures for the sub-45 nm roadmap.*

BERNIN, France — July 15, 2008 — Soitec (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) wafers and other engineered substrates used in the microelectronics industry, has announced today a new generation of advanced substrates that support all the applications and architectures on the industry's sub-45 nm roadmap. New solutions such as ultra-thin top silicon and ultra-thin Buried OXide (BOX) give device architects and designers complete flexibility in their choice of substrates for partially depleted (PD) and fully-depleted (FD) devices, including multi-gate transistor architectures (FinFET, Trigate).

The new generation of substrates is built on the highly successful 300mm Unibond™ XUT+ wafers, which are currently shipping to leading customers for the PD 45-nm logic market, and which are also under qualification or sampling with other customers in a variety of system-on-chip applications.

“To make strategic choices for 32 nm and beyond, Soitec customers now have a full range of options at their disposal,” notes Paul Boudre, Soitec's COO. “Device architects can leverage substrate design in their solutions for scaling, low power, and greatly reduced threshold voltage variability, thus ensuring SRAM scalability, and in particular stability at low operation voltages and significantly improved soft error rate. This is a major advantage for IC design today. In addition, CMOS process simplifications, and advanced SOI memory solutions—like single transistor body cell or ZRAM— result in a lower cost-of-ownership for SOI ICs.”

This new generation of substrates fabricated using the company's patented Smart Cut™ process is designed to meet the most advanced requirements in terms of defectivity, flatness and SOI thickness control of up to  $\pm 10$  Angstroms (Å). The top silicon layer of these wafers is available in thicknesses ranging from just 20 nm up to 110 nm, while the BOX can be as thin as 10 nm. Options are also available like High Resistivity substrate and strained SOI.

Visit Soitec in San Francisco, at Semicon West, North Hall, booth #5428.

### **About the Soitec Group:**

The Soitec Group is the world's leading innovator and provider of the engineered substrate solutions that serve as the foundation for today's most advanced microelectronic products. The group leverages its proprietary Smart Cut™ technology to engineer new substrate solutions, such as silicon-on-insulator (SOI) wafers, which became the first high-volume application for this proprietary technology. Since then, SOI has emerged as the material platform of the future, enabling the production of higher performing, faster chips that consume less power.

Today, Soitec produces more than 80 percent of the world's SOI wafers. Headquartered in Bernin, France, with two high-volume fabs on-site, Soitec has offices throughout the United

States, Japan and Taiwan, and a new production site in the process of customers' qualification in Singapore.

Two other divisions, Picogiga International (Les Ulis) and Tracit Technologies (Bernin), complete the Soitec Group. Picogiga focuses on delivering advanced substrates solutions, including III-Vs epiwafers and gallium nitride (GaN)-based wafers, to the compound material world for the manufacture of high-frequency electronics and other optoelectronic devices. Tracit, on the other hand, focuses on thin-film layer transfer technologies used to manufacture advanced substrates for power ICs and microsystems, as well as generic circuit transfer technology for applications such as image sensors and 3D-integration. Shares of the Soitec Group are listed on Euronext Paris. For more information, visit [www.soitec.com](http://www.soitec.com).

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