Soitec ultra-thin SOI substrates enabling FD-SOI technology

July, 2015
Agenda

• FD-SOI: Background & Value Proposition
Today Ultra-mobile & Connected Consumer

At Any Time

With Anyone

Anywhere
(any place, any service, any network)

With Anything

→ Intensified Challenges

Outstanding Performance

Longer battery life

Optimized cost
FD SOI – Performance, Power & Cost Efficiency

3 GHz demo on ARM-based

Smartphone on 28nm FDSOI

Source: ST

28nm FD-SOI provides « 20nm performance at 28nm cost »,
Quote from FD-SOI foundry offering slides shown on Samsung booth, DAC2014

+5h web browsing

Thermal camera on smartphone
Apps Proc. Gets Hot (High Pwr Cons.) | Apps Proc. Stays Cool

Dual A9 both running at 1.85GHz

Source: ST

Cost per Million Gates ($)

<table>
<thead>
<tr>
<th>90nm</th>
<th>65nm</th>
<th>40nm</th>
<th>28nm</th>
<th>20nm</th>
<th>16/14nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>0.026</td>
<td>0.064</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FD-SOI</td>
<td></td>
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</table>

Good trend for FDSOI
Moore’s Law

Wrong trend (Higher integration = higher cost)

Source: IBS

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Conventional silicon technology not suitable anymore

Moore’s Law:

- For similar chip cost:
  - More functionalities (more transistors per chip)
  - Less power per transistor
  - Faster processing

Planar bulk CMOS reaching its limits at 20nm, Can’t go further:

- **Technical** challenges
  (leakage, variability and short channel effects)

- **Cost**-efficiency challenges
Two Scaling Paths for Alternate Device Architecture: Planar FD-SOI or Multi-Gate Transistor

**Planar Bulk**

- **Transistor Cross-section**
- **Fully Depleted Technologies**
- **Not beyond 20nm**

- Behavior controlled by doping

**Planar FD-SOI**

- Planar transistor architecture
- Evolution

**FinFET**

- 3-D transistor architecture
- Revolution

- New paradigm: Behavior controlled by silicon geometry
FD-SOI story: visionary innovations and partnerships

2005
Substrate Supply

2005
Research Institute

2008
Advanced R&D

2010
Industrial Partner

2014
Open foundries

2015
Products on the market

Smart Cut™ technology

FD-SOI substrates

FD-SOI processed wafer with multiple raw dice per wafer

FD-SOI transistor

Silicon die with millions of transistors

2005 Substrate Supply

2005 Research Institute

2008 Advanced R&D

2010 Industrial Partner

2014 Open foundries

2015 Products on the market

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Planar FD roadmap: Scalable down to 10nm

Source: L. Mallier (Leti) at Leti Innovation Days, June 25 2013
FD-SOI is excellent for mobile …and many other applications

FD-SOI Application Benefits

**Consumer**
- Optimized SoC integration (Mixed-signal & RF)
- Energy efficient SoC in all thermal conditions
- Optimized leakage in idle mode

**Infrastructure Networking**
- Energy efficient **multicore**
- Effective DVFS
- Excellent performance on **memories**

**Internet of Things**
- Ultra-low voltage operation
- Highly Scalable operation
- Efficient **RF and analog** integration

**Automotive**
- Well-managed leakage in high temperature environment
- High reliability thanks to highly-efficient memories

Source: ST, SOI Forum, San Francisco Feb 2015
Agenda

1. FD-SOI: Background & Value Proposition

2. The FD-SOI ecosystem & markets
A full FD-SOI ecosystem is now in place

May 2014 - Samsung to provide 28nm FD-SOI as open foundry, Press release here
May 2014 - Cadence ready to provide 28nm FD-SOI physical IP blocks, Press release here
June 2014 - Synopsys to collaborate with Samsung, ST to accelerate 28nm FD-SOI adoption, Press release here
June 2015 - GlobalFoundries FD-SOI technology webinar here
28FD-SOI: Cost effective low power solution for long lived 28nm

Kelvin LOW
Sr Director, Foundry Marketing
27 FEB 2015

28FDSOI Reliability Summary

- WLR Qualification: Completed in Sep 2014

<table>
<thead>
<tr>
<th>Items</th>
<th>Device</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDBB</td>
<td>Core (SG)</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>IO (EG)</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>BTI</td>
<td>Core (SG)</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>IO (EG)</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td>HCI</td>
<td>Core (SG)</td>
<td>Pass</td>
<td>Pass</td>
</tr>
<tr>
<td></td>
<td>IO (EG)</td>
<td>Pass</td>
<td>Pass</td>
</tr>
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28FDSOI Low Vdd superiority

Ideal for battery operated ultra low power applications (IoT/wearable)
GlobalFoundries FD-SOI webinar June 2015

Summary

- FD-SOI is a cost effective alternative to FinFET
- Ideal for applications like IoT, consumer, and low-end mobility
- Integrates logic, RF and eNVM on the same die for reduced power and system cost
- Optional Body Biasing for flexible tradeoff of performance vs. power
- Leverages bulk digital design flows and existing EDA tools
- Strong industry support and scalable to 10nm – ensuring that FD-SOI has a bright future

Source: GF FD-SOI Technology Webinar, June 2015, available here
Examples of wearable application:
FD-SOI enables added functionality at ULP for IoT applications

x20 Power Consumption Improvement
On-Chip enabled functionality (RF, logic and SRAM) operating at 0.6V, instead of 1.1V

FD-SOI benefits for automotive applications

Example: Automotive Video analytics processor

FD-SOI Soft Error Rate (SER) allows for less overhead in memories for error correction.

Power limit for windscreen-mounted video analytics systems ~3W

Source: ST, SOI Forum, San Francisco, Feb2015
SOI wafer supply ensured

300mm SOI starting wafer production sites, Worldwide:
Soitec ~70% today

800 Kwfrs/yr capacity, fully installed, for PD- and FD-SOI. Full conversion to FD in progress.

1 Mwfrs/yr capacity when fully installed. Qualified for FD-SOI. Ready to ramp according to demand in well under a year.

Close to 2 Mwfrs/yr capacity readily available when needed.
Smart Cut™ Alliance – A model for growth
Agenda

1. FD-SOI: Background & Value Proposition
2. The FD-SOI ecosystem & Markets
3. Soitec’s ultra-thin SOI wafers
Soitec Fully-Depleted Product Roadmap

Target node | 28 nm “28FD” | 20/14 nm “14FD” | 10 nm “10FD” | 7 nm and beyond

<table>
<thead>
<tr>
<th>FD-2D</th>
<th>Box thickness</th>
<th>Top Si unif</th>
<th>Top Si thickness</th>
<th>Top Si stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD-3D</td>
<td>Top Si stress</td>
<td>Top Si thickness</td>
<td>Top Si stress</td>
<td>Top Si stress</td>
</tr>
</tbody>
</table>

Available upon request

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During Tech. Dev Phase, early samples are available for selected customers
Simpler process with FD-SOI: Transistor channel pre-defined by substrate

- FD-2D wafers provide excellent control of transistor geometry
  - To make the best of FD technology

**FD-SOI transistor**

**Critical dimension:**
- Top Si thickness

**Enables:**
- No complex channel doping required
- Critical body geometry pre-defined by top silicon
- Simplified CMOS process
Top silicon uniformity: the exceptional made industrial

Silicon thickness uniformity is guaranteed to within just a few atomic layers:

Top Si uniformity = +/-5 Å at all points on all wafers, equivalent to +/- 5 mm over 3,000 km (corresponds to ~ +/-0.2 inches over the distance between San Francisco and Chicago)

Soitec FD-2D wafer

San Francisco - Chicago ~ 2,988 km (1,857 mi)
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4. Cost Aspects
IBS’s view on FD-SOI market potential

FD SOI MARKET (CONTINUED)

WAFER VALUE

PRODUCT VALUE

FD SOI MARKET HAS GOOD GROWTH POTENTIAL
Industry Analyst IBS demonstrates FD-SOI competitive advantage

"FD-SOI offers best power / performance / cost trade-off for high volume portable applications"  
- H Jones, IBS

- Several studies (IC Knowledge, ST) reach similar conclusions: FD-SOI is extremely cost-competitive vs. any alternative
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4. Cost Aspects
5. Take-Aways
Take-Aways

- **28nm FD-SOI:**
  outstanding power/performance for the cost of standard 28nm low-power CMOS

- ‘14FD’ / 20nm FD-SOI:
  a compelling, cost-effective alternative to FinFET

- Tight wafer specifications are fully met by Soitec in a production environment

- Open foundry offering for FD-SOI at Samsung and GF

- Full ecosystem is in place for high-volume markets
  from wafer supply through IP & design environment to foundry manufacturing
Summary - FD-SOI: confirmed adoption

**Strong competitive advantages**

Best Performance/Power/Cost
DAC 2014

- 20nm
- 14 FinFET
- 28LPP
- 28 FD-SOI
- 14 FD-SOI

A rapidly growing ecosystem and products announcements

"There is an opportunity to turn SOI from niche into mainstream."
Kevin Low, Samsung senior director foundry marketing

"For cost-sensitive markets with more analog integration, FD-SOI is the right solution."
Jamie Schaeffer, GF product line manager

A considerable potential

28nm FD-SOI potential

"The 28nm technology will represent approximately 4.3 million wafers in 2017 and FD-SOI could capture at least 25% of the market."
H. Jones, IBS

FD-SOI for **COST & POWER SENSITIVE MARKETS**: automotive, IoT, mobile and networking

New products under qualification using FD-SOI
Thank You