SOITEC ANNOUNCES SIGNIFICANT COLLABORATION TO DEVELOP WAFER-LEVEL 3D INTEGRATION TECHNOLOGY

Bernin, France, July 14, 2009 — The Soitec Group (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) and other engineered substrates for the microelectronics industry, announced today that it has entered into collaboration with IBM to pioneer 22-nanometer (nm) node and beyond silicon wafer substrate and bonding techniques that will enable wafer-level, three-dimensional (3D) integration technology for next-generation integrated circuits (ICs). The two companies have been working together for many years to improve the design and specifications of advanced silicon wafer substrates to meet the needs of IBM's manufacturing roadmap.

The objective of this new collaboration is to develop highly flexible and cost-effective solutions for wafer-to-wafer stacking, a semiconductor technology designed to yield ICs with faster speeds and higher performance. In joining IBM's 3D integration effort, Soitec will leverage its Smart Stacking™ technology and all of its wafer-level bonding expertise including oxide-to-oxide and metal-to-metal molecular bonding—developed in collaboration with CEA/Leti (the Electronics and Information Technology Laboratory of the of the French Atomic Energy Commission).

"This collaboration with Soitec is another step in IBM's drive to accelerate 3D integration technology, and reinforces the expanding IBM ecosystem of leading companies and research organizations that are working together to achieve significant advances in semiconductor and packaging technology," said Dr. Gary Patton, Vice President, Semiconductor Research and Development Center, IBM. "Through these collaborations, IBM intends to accelerate the development of emerging 3D integration technology and demonstrate the possibilities of achieving higher circuit densities, faster speeds and lower power usage with this vertical integration approach."

"Soitec has continuously supported IBM's development programs over the past 15 years with our SOI and other engineered substrates. We expect this new collaboration with IBM will help solve the challenges that IBM is addressing through its 3D program," said Carlos Mazuré, CTO of Soitec.

About the Soitec Group:

The Soitec Group is the world's leading innovator and provider of the engineered substrate solutions that serve as the foundation for today's most advanced microelectronic products. The group leverages its proprietary Smart Cut™ technology to engineer new substrate solutions, such as silicon-on-insulator (SOI) wafers, which became the first high-volume application for this proprietary technology. Since then, SOI has emerged as the material platform of the future, enabling the production of higher performing, faster chips that consume less power.

Today, Soitec produces more than 80 percent of the world's SOI wafers. Headquartered in Bernin, France, with two high-volume fabs on-site, Soitec has offices throughout the United States, Japan and Taiwan, and a new production site in the process of customers' qualification in Singapore.

Two other divisions, Picogiga International (Les Ulis) and Tracit Technologies (Bernin), complete the Soitec Group. Picogiga delivers advanced substrates solutions, including III-V epiwafers and gallium nitride (GaN) wafers, to the compound material world for the manufacture of high-frequency electronics and other optoelectronic devices. Tracit, on the other hand, provides thin-film layer transfer technologies used to manufacture advanced substrates for power ICs and microsystems, as well as generic circuit transfer technology Smart Stacking for applications such as image sensors and 3D-integration. Shares of the Soitec Group are listed on Euronext Paris. For more information, visit www.soitec.com.

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