IC KNOWLEDGE’S COST MODELING OF SEMICONDUCTOR MANUFACTURING SHOWS FULLY DEPLETED SILICON-ON-INSULATOR TECHNOLOGY TO BE THE MOST COST-EFFECTIVE APPROACH AT THE 22 NM NODE

FD-SOI Determined to Be More Economical Than Planar Bulk Silicon CMOS Processing

Georgetown, Mass., July 12, 2011 — Research firm IC Knowledge LLC has completed a comprehensive cost analysis that determines fully depleted silicon-on-insulator (FD-SOI) wafers offer the global semiconductor industry the most cost effective solution compared to bulk silicon for processing semiconductor devices at the next-generation 22 nm technology node and beyond.

“FD-SOI offers the potential for significant process simplification, making it cost competitive while simultaneously offering performance improvements over bulk silicon,” said Scotten W. Jones, president of IC Knowledge. “The ability to use fewer steps enables FD-SOI’s greater cost efficiency.”

In particular, FD-SOI processing dramatically decreases the number of implant masks and implant steps needed. Although implant-related costs are relatively low, FD-SOI’s fewer total processing steps offers a simpler overall process flow.

“Fully depleted SOI is the key,” Jones added.

In conducting its analysis, IC Knowledge worked with a wafer-processing consultant and Soitec, the world leader in SOI wafer manufacturing, to define three sample process flows representative of state-of-the-art industry practices for the 22 nm node: one planar bulk CMOS and two versions of FD-SOI – with implanted source/drain or with in-situ doped source/drain.

All process flows assumed three threshold voltages, dual gate oxides and suitability for system-on-a-chip (SOC) applications. The bulk CMOS process assumed a suite of mobility-enhancing stressors. The two FD-SOI process flows, on top of relevant mobility-enhancing stressors, also assumed multiple features such as n+ and p+ back-gates and n-well and p-well implants under the buried oxide (BOx) layer, access to the n-well and p-well, two shallow-trench isolation depths and electro-static discharge
(ESD) devices in a bulk area. The same gate integration schemes (gate-last high-\(k\) metal gate) and number of metal layers (eight) were assumed in all scenarios. For SOI, a volume pricing of $500 per starting wafer was added. For bulk silicon, an aggressive price of $130 per (epi) starting wafer was selected.

IC Knowledge then utilized its Strategic Cost Model to evaluate how each process flow would perform in a Taiwanese wafer fab producing 30,000 wafers per month in the 2012 timeframe. The scenario generator considered the costs of starting wafers, direct and in-direct labor, depreciation of the wafer fab, equipment maintenance, monitor wafers, facilities such as electricity, and consumables such as reticle sets, gases and chemicals. Calculations of the cost per wafer yielded used in the model have been validated by IC Knowledge using wafer cost data collected from fabs throughout the semiconductor industry.

The Strategic Cost Model’s analysis determined that the most economical yielded-wafer cost was achieved by FD-SOI processing with in-situ doped source/drain, at approximately $3,000 per wafer. Furthermore, both versions of FD-SOI were determined to be extremely cost competitive compared to bulk CMOS. The study found only about one percent difference in the cost of yielded processed wafers produced by the second FD-SOI option – with implanted source/drain – and bulk CMOS.

Because this analysis is strictly based on costs, IC Knowledge’s findings do not address FD-SOI’s superiority to bulk silicon in producing semiconductors with lower leakage and faster processing speeds or compare the performance of SOI and bulk silicon in processing multi-gate transistors at the 22 nm node and beyond.

The report is available on:  

About IC Knowledge:
IC Knowledge is the world leader in cost modeling for the semiconductor and MEMS industries. In addition to custom projects IC Knowledge offers a variety of cost modeling tools as well as reports, databases and forecasts. IC Knowledge’s customers include leading semiconductor and MEMS companies, OEMs, fabless design houses, system manufacturers, industry analysts and many others. For more information please visit www.icknowledge.com.

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