



SOITEC LEVERAGES CORE TECHNOLOGIES TO ADDRESS WAFER-LEVEL 3D INTEGRATION

Company's extensive and flexible platform is ideally suited for maximizing 3D integration's advantages in IC performance, power, size and manufacturing cost

San Francisco, July 13, 2009 — The Soitec Group (Euronext Paris), the world's leading supplier of silicon-on-insulator (SOI) and other engineered substrates for the microelectronics industry, announced today its strategy for solving technology challenges in the growing wafer-level 3D integration market with a family of proven processes and engineered substrates. The company has the combination of core technology know-how in wafer bonding and stacking, manufacturing infrastructure and high-volume experience, as well as strong IP to develop the building blocks required for wafer-level 3D integration. Soitec's 3D technology strategy is built on three pillars: Low-temperature Smart Cut™ technology, Smart Stacking™ technology and metal-to-metal direct bonding, currently in development.

"3D integration and wafer-level packaging technologies are promising and fast-growing segments of tomorrow's semiconductor industry. We expect 3D integrated semiconductors to grow at a CAGR of 50 to 60% during the period 2008 to 2015, mainly driven by memories, image sensors, MEMS, analog and CMOS logic applications," said Jérôme Baron, principal analyst at *Yole Développement*. "Despite the current economic downturn, the worldwide R&D activities linked to 3D integration innovation have reached unprecedented levels."

"We are working on making 3D technologies feasible and cost effective with an extensive and flexible offer. At the wafer level, both our Smart Stacking and Smart Cut technologies add significant value to 3D integration," said André-Jacques Auberton-Hervé, president of the Soitec Group. "And when SOI wafers are used for CMOS processing, as demonstrated with imagers, end products are benefiting from higher yields and improved reliability."

Smart Stacking technology enables wafer-to-wafer level stacking of partially or fully processed circuits. The technique uses low-temperature oxide-oxide molecular bonding with specific surface conditioning, and high-precision wafer thinning. The low-stress wafer bonding process remains compatible with future requirements for submicron alignment

accuracy. This technology is adapted for advanced semiconductor applications such as Back-Side Illumination (BSI) image sensors as well as via last 3D integration approaches. Using SOI as starting material, Soitec's technologies allow the successful stacking of extra-thin layers needed to achieve the highest through-silicon-via (TSV) interconnect densities.

Soitec's low-temperature Smart Cut process uses oxide-oxide molecular bonding and atomic-level cleaving to transfer mono-crystalline silicon films as thin as 0.1 micron onto partially or fully processed wafers. On this new material layer, a second level of devices can be processed and this integration can be repeated in an iterative mode. Transferring an extremely thin layer enables higher interconnect density, higher signal throughput and simpler TSV processing. Benefits include increased computing bandwidth, lower overall manufacturing cost, and power savings due to the reduced wiring distance between connected devices. This final benefit is well suited for producing advanced memory or CMOS logic 3D IC systems.

Additionally, Soitec's R&D work in metal-to-metal bonding in partnership with CEA/Leti (the Electronics and Information Technology Laboratory of the French Atomic Energy Commission) plays a key role in the company's 3D integration strategy. This approach presents the advantages of applying no additional pressure on the bonding stack and a lower thermal budget to guard against distortion and misalignment. The main application is in creating interconnections in the 3D stack during bonding.

At SEMICON West, July 14-16 in San Francisco, visit Soitec in booth #5448 in North Hall.

About the Soitec Group:

The Soitec Group is the world's leading innovator and provider of the engineered substrate solutions that serve as the foundation for today's most advanced microelectronic products. The group leverages its proprietary Smart Cut™ technology to engineer new substrate solutions, such as silicon-on-insulator (SOI) wafers, which became the first high-volume application for this proprietary technology. Since then, SOI has emerged as the material platform of the future, enabling the production of higher performing, faster chips that consume less power.

Today, Soitec produces more than 80 percent of the world's SOI wafers. Headquartered in Bernin, France, with two high-volume fabs on-site, Soitec has offices throughout the United States, Japan and Taiwan, and a new production site in the process of customers' qualification in Singapore.

Two other divisions, Picogiga International (Les Ulis) and Tracit Technologies (Bernin), complete the Soitec Group. Picogiga delivers advanced substrates solutions, including III-V epiwafers and gallium nitride (GaN) wafers, to the compound material world for the manufacture of high-frequency electronics and other optoelectronic devices. Tracit, on the other hand, provides thin-film layer transfer technologies used to manufacture advanced substrates for power ICs and microsystems, as well as generic circuit transfer technology, Smart Stacking for applications such as image sensors and 3D-integration.

Shares of the Soitec Group are listed on Euronext Paris. For more information, visit www.soitec.com.

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